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Sheet 1 of 1

	Complete if Known
Application Number	10/033,716
Filing Date	12/28/2001
First Named Inventor	Robert W. Bower
Art Unit	8633
Examiner Name	S. A. Gebremariam
Attorney Docket Number	BOW5075.04A

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Ellis, R. K. et al. "Electron Tunneling in Non-planar Floating Gate Memory Structure", IDEM, 1982, pp. 749-752.	
		Shealy, J.R. et al. "Direct band gap structures on nanometer-scale, micromachined silicon tips", Appl. Phys. Lett. Vol. 70, No. 25, June 1997, pp. 3458-3460.	
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		Sze, S.M. "Physics of Semiconductor Devices", Wiley-Interscience, ISBN 0471056618, 1981, pp. 46, 47, 690, 691.	
		Wegener, H.A.R. et al. "The prediction of textured poly floating gate memory endurance", 23rd annual Proceedings on Reliability Physics, 1985, pp. 11-17.	

Examiner Signature		Date Considered	7/7/04

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